CLAIMS

We claim:

1. A step down voltage regulator comprising devices designed to operate over a maximum rated voltage lower than the supply voltage, comprising:

an output regulation device coupled to the supply voltage and an output; and

an output device protection circuit responsive to the supply voltage and the output to ensure that the maximum rated voltage of the output regulation device is not exceeded.

2. The regulator of claim 1 wherein the output regulation device comprises a p-channel transistor.

3. The regulator of claim 2 wherein the p-channel transistor has an operating maximum rated voltage in a range of 2.7 – 3.3 volts and the supply voltage is in a range of 4.4 – 5.25 volts.

4. The regulator of claim 2 wherein the output device protection circuit includes a gate-source protection component.

5. The regulator of claim 2 wherein the output device protection circuit includes a gate-drain protection component.

6. The regulator of claim 5 wherein the gate-drain protection component includes a gate hold-down circuit limiting the voltage of the gate until the regulator output reaches a minimum voltage.

7. The regulator of claim 6 wherein the minimum voltage is 3.3 volts.

8. The regulator of claim 6 wherein the hold-down circuit includes an output controlled device.

9. The regulator of claim 8 wherein the output controlled device is a p-channel transistor.

10. The regulator of claim 9 wherein the hold-down circuit further includes an n-channel device coupled to the source of the p-channel device.

11. The regulator of claim 4 wherein the gate-source protection component includes an n-channel transistor having a drain coupled to the supply voltage and a source coupled to a gate of the output device.

12. A voltage regulator supplying an output voltage lower than a supply voltage, comprising:

an output device designed to operate at a maximum rated voltage lower than the supply voltage; and

an output device protection circuit regulating a gate voltage of the output device relative to a drain load and a source voltage on the output device so as to not exceed the maximum rated voltage.

13. The regulator of claim 12 wherein the output device comprises a p-channel transistor.

14. The regulator of claim 13 wherein the p-channel transistor has an operating maximum rated voltage in a range of 2.7 – 3.3 volts and the supply voltage is in a range of 4.4 – 5.25 volts.

15. The regulator of claim 12 wherein the output device protection circuit includes a gate hold-down circuit limiting the voltage of the gate until the regulator output reaches a minimum voltage.

16. The regulator of claim 15 wherein the minimum voltage is 3.3 volts.

17. The regulator of claim 15 wherein the hold-down circuit includes an device controlled by the output load of the regulator.

18. The regulator of claim 17 wherein the output controlled device is a p-channel transistor.

19. The regulator of claim 15 wherein the hold-down circuit further includes an n-channel device coupled to the source of the p-channel device.

20. The regulator of claim 19 wherein the output device protection circuit includes an n-channel transistor having a drain coupled to the supply voltage and a source coupled to a gate of the output device.

21. A memory system including a control path and a data path to a host device, and receiving a supply voltage from the host device, comprising:

a voltage regulator including

a voltage input coupled to the supply voltage;

an output device operating at a maximum rated voltage less than the supply voltage and coupled to a regulator output; and

a protection circuit coupled to the voltage input and the output device, including an output device gate control, the protection circuit comprising a plurality of output control devices operating at maximum rated voltages less than the voltage provided by the host at the input.

22. The memory system of claim 21 wherein the protection circuit regulates a gate voltage of the output device relative to a regulator output.

23. The memory system of claim 22 wherein the regulator output is the drain of the output device.

24. The memory system of claim 21 wherein the output device comprises a p-channel transistor.

25. The memory system of claim 24 wherein the p-channel transistor has an operating maximum rated voltage in a range of 2.7 – 3.3 volts and the supply voltage is in a range of 4.4 – 5.25 volts.

26. The memory system of claim 21 wherein the minimum voltage is 3.3 volts.

27. The memory system of claim 21 wherein the hold-down circuit includes an device controlled by the output load of the memory system .

28. The memory system of claim 27 wherein the output controlled device is a p-channel transistor.

29. The memory system of claim 31 wherein the hold-down circuit further includes an n-channel device coupled to the source of the p-channel device.

30. The memory system of claim 29 wherein the output device protection circuit includes an n-channel transistor having a drain coupled to the supply voltage and a source coupled to a gate of the output device.

31. The memory system of claim 21 wherein the output device protection circuit includes a gate hold-down circuit limiting the voltage of the gate until the memory system output reaches a minimum voltage.

32. A method for operating a voltage regulator in a memory system, comprising:

providing a voltage regulator having an input and an output, and including a plurality of devices operating at a maximum rated voltage less than the voltage provided at the input; and

controlling the gate voltage of the output device responsive to a load on the regulator output, so that the maximum rated voltage is not exceeded.

33. The method of 32 wherein said step of controlling includes regulating a gate voltage of the output device relative to a regulator output.

34. The method of claim 33 wherein the regulator output is the drain of the output device.

35. The method of claim 34 wherein the output device has an operating maximum rated voltage in a range of 2.7 – 3.3 volts and the supply voltage is in a range of 4.4 – 5.25 volts.

36. The method of claim 32 wherein the minimum voltage is 3.3 volts.

37. The method of claim 32 wherein the controlling step includes controlling a device controlled by the output load of the regulator.

38. The method of claim 27 wherein the output controlled device is a p-channel transistor.

39. The method of claim 31 wherein the controlling step includes regulating an n-channel device coupled to the source of the p-channel device.

40. The method of claim 31 the controlling step includes a limiting the voltage of the gate until the regulator output reaches a minimum voltage.

41. A peripheral device for a host system including a voltage regulator circuit, comprising:

a functional component;

a voltage regulator having an supply voltage input and an output;

an output regulation device coupled to the supply voltage and the output; and

an output device protection circuit responsive to the supply voltage and the output to ensure that the maximum rated voltage of the output device is not exceeded.

42. The peripheral device of claim 41 wherein the functional component is a memory system.

43. The peripheral device of claim 42 wherein the memory system includes a controller and a memory array.

44. The peripheral device of claim 42 wherein the memory system is a pc card.

45. The peripheral device of claim 42 wherein the memory system is compact flash card.

46. The peripheral device of claim 42 wherein the memory system is a secure digital card.

47. The peripheral device of claim 42 wherein the memory system is a smart media card.

48. The peripheral device of claim 42 wherein the memory system is a memory stick.

49. A memory system, comprising:

a controller;

a memory array; and

a voltage regulator including a plurality of devices operating at maximum rated voltages less than a supply voltage and having an output regulation device coupled to the supply voltage and an output, and an output device protection

circuit responsive to the supply voltage and the output to ensure that the maximum rated voltage of the output device is not exceeded.